WHAT IS CLAIMED IS:

1. A static semiconductor memory device, comprising:

a number M × N (M: integer not less than 2; N: integer not less than 2) of memory blocks each of which include a number 8 × M of horizontal memory cells arranged in eight rows by M columns and which are arranged in M rows by N columns,

a word line provided corresponding to each memory cell row of each memory block,

first and second bit lines provided in common for the number M of memory block rows so as to correspond to each memory cell column,

first and second bit line signal input/output lines provided corresponding to each memory block and connected to the first and second bit lines of a predetermined pair of the corresponding M pairs of the first and second bit lines, respectively,

first and second data input/output lines provided corresponding to each memory block row for inputting/outputting data of the corresponding memory block row,

first and second power supply lines provided corresponding to each memory block row,

a global word line provided corresponding to each memory block row for selecting the corresponding memory block row,

a global column selecting line provided in common for the number M × N of memory blocks so as to correspond to each memory cell column for selecting the corresponding memory cell column,

a selection circuit responsive to an address signal for driving said word line, said global word line and said global column selecting line to select any one memory block of said number M × N of memory blocks and any one memory cell of the number 8 × M of memory cells belonging to the memory block,

a write/read circuit for writing/reading data of said memory cell, and

a gate circuit for coupling a memory cell selected by said selection circuit to said write/read circuit through said first and second bit lines, said

first and second bit line signal input/output lines and said first and second data input/output lines, wherein

in each memory block column, the M sets of said first and second bit line signal input/output lines, said first and second data input/output lines, said first and second power supply lines, said global word lines and said global column selecting line are arranged above the number M of memory blocks respectively, and extend in the same direction as that of said word line,

each set of said first and second bit line signal input/output lines, said first and second data input/output lines, said first and second power supply lines and said global word lines and said global column selecting lines are arranged above eight memory cell rows included in the corresponding memory block, respectively,

said first power supply line is arranged between said first and second bit line signal input/output lines and said first and second data input/output lines, and said global word line, and

said second power supply line is arranged between said first and second bit line signal input/output lines and said first and second data input/output lines, and said global column selecting line.

2. The static semiconductor memory device according to claim 1, wherein the M pairs of the first and second power supply lines are provided corresponding to the M pairs of the first and second bit lines in each memory block column, and which further comprises:

a bit line load circuit provided corresponding to each memory block for applying a power supply potential applied through the corresponding first power supply line to the corresponding first and second bit line signal input/output lines, and

a third power supply line provided corresponding to each of the first and second bit lines for applying said power supply potential applied through the corresponding second power supply line to each corresponding memory cell.

3. The static semiconductor memory device according to claim 2, wherein a redundant system of replacing a defective memory cell row or column by a spare memory cell row or column is adopted, and which further comprises:

a first switching element provided corresponding to each first power supply line and having one electrode connected to the corresponding first power supply line and the other electrode receiving said power supply potential,

a second switching element provided corresponding to each second power supply line and having one electrode connected to the corresponding second power supply line and the other electrode receiving said power supply potential, and

a first program circuit provided corresponding to each of the first and second power supply lines and including a first fuse which is to be blown when the corresponding memory cell column is defective, and responsive to blowing of the first fuse for rendering the corresponding first and second switching elements non-conductive.

4. The static semiconductor memory device according to claim 3, wherein

said selection circuit includes:

a global column decoder responsive to said address signal for selecting any one global column selecting line of the number M of global column selecting lines to bring the global column selecting line to a selected level, and

a global row decoder responsive to said address signal for selecting any one global word line of the number M of global word lines to bring the global word line to the selected level, and

said first program circuit further controls said global column decoder to fix the corresponding global column selecting line at a non-selected level in response to said first fuse being blown.

5. The static semiconductor memory device according to claim 4,

wherein other part of said first program circuit than said first fuse and said global column decoder are arranged between said first fuse and said memory block.

6. The static semiconductor memory device according to claim 4, further comprising a second program circuit provided corresponding to each global word line and including a second fuse which is to be blown when the corresponding memory block row is defective, and responsive to blowing of the second fuse for controlling said global row decoder to fix the corresponding global word line at the non-selected level.

7. The static semiconductor memory device according to claim 6, wherein other part of said first and second program circuits than said first and second fuses, said global column decoder and said global row decoder are arranged between said first and second fuses and said memory block.